

REMARKS

Interview Summary: On November 2, 2006, LeRoy Maunu (Reg. No. 35,274) discussed with Examiner Colin the rejection of claims 1 and 12 under 35 USC §112 and the rejection of claim 1 under 35 USC §103(a). No agreement was reached as to the allowability of the claims.

Claim 1 is amended to clarify the invention and for purposes of expediting prosecution. New claim 44 is added to further specify the generating of the ratio (see paragraph [0031], for example). Applicant maintains the traversals of the rejections set forth in all prior Office Actions and incorporates herein the arguments made in response to those rejections as set forth in previously filed amendments and responses. Claims 1-4, 7, 12-13 15, 21, and 44 remain for consideration and are thought to be allowable over the cited art. Reconsideration and allowance are respectfully requested.

The rejection of claims 1 and 12 under 35 USC §112, first paragraph, is respectfully traversed. The rejection is moot, however, in view of the amendments to the claims.

The Office Action does not establish that Claims 1-4, 7, 12-13, 15 and 21 are unpatentable under 35 USC §103(a) over "Erickson" (U.S. Patent No. 5,970,142 to Erickson) in view of "Mos" (US Patent No. 6,260,146 to Mos. et al.). The rejection is respectfully traversed because the Office Action does not show that all the limitations are suggested by the references and does not provide a proper motivation for modifying the teachings of Erickson with teachings of Mos.

The Office Action is incorrect in the assertion that Erickson's teachings col. 2, l. 30-31 and col. 4, l. 44-65 suggest the limitations of a fingerprint that represents an inherent manufacturing process characteristic unique to the FPGA. It is respectfully submitted that both sections appear to generally teach pseudo-randomly generating a key. There is no apparent suggestion of how the key generation relates to any inherent manufacturing process characteristic unique to the FPGA. Nor does the Office Action indicate how the teachings could be construed as such. Therefore, these limitations are not shown to be suggested by Erickson. If the rejection is

maintained, an explanation is requested as to how these teachings might be understood to suggest these specific claim limitations.

The Office Action is also incorrect in the assertion that Mos suggests counting a first number of oscillations of a first oscillator on the FPGA during a predetermined time interval, counting a second number of oscillations of a second oscillator on the FPGA during the predetermined time interval, and generating a ratio between the first number and second number of oscillations, wherein the ratio is the fingerprint.

In order to provide a system that is capable of authenticating information stored on a magnetic medium in a manner that is unaffected by the speed of the medium relative to the reader, Mos discloses an approach for determining the distance between transitions from a first logical state to a second logical state stored on a medium (Abstract, col. 3, l. 3-10). The approach is useful for measuring deviations in spacing between logical transitions used to represent information stored on a medium with an encoding scheme in which logical transitions must occur at regular intervals (col. 5, l. 15-18).

Mos does not suggest two oscillators. Rather, Mos appears to use a single processor 404 to generate multiple count values (col. 8, l. 20). Thus, Mos' single processor suggests a single oscillator. Mos further uses a combination of a current amplifier, coils, and zero crossing detector to generate a signal indicative of a transition on the medium (col. 8, l. 5-18).

Furthermore, the various counts accumulated in Mos demonstrate that counts of two oscillators are not accumulated. Since Mos counts transitions on a storage medium, the counts depend on orientation of the lines of flux on the medium and the velocity of the medium relative to the read apparatus (col. 9, l. 16-17). A counter is started in response to a zero crossing detector detecting a signal transition resulting from a change in direction of lines of flux on the medium (col. 8, l. 3-39). There are a leading and a trailing read apparatus, each having a zero crossing detector. The elapsed count value represents the distance between logical transitions on each of the signals output from the read apparatus (col. 8, l. 40-43). Distances measured between the leading and trailing read apparatus for the same transition are "reference values" and stored in a reference FIFO, and distances measured by the leading read

apparatus for adjacent transitions are "jitter values" and stored in a jitter FIFO (col. 8, l. 46-52). Mos' other counter, the Half Bit Cell Count (HBCC) increments at each half bit cell such that each half bit cell on the medium can be uniquely identified. The reference values and jitter values are associated with the HBCCs indicating a location on the medium (col. 8, l. 66 – col. 9, l. 12). Thus, Mos's count values represent distances between logical transitions on a storage medium, not oscillations of an oscillator during a time interval.

Mos' ratio does not suggest the claimed ratio. To compensate for variations in the velocity of the storage medium, Mos suggests a jitter ratio. Mos' jitter ratio is a quotient of the jitter value divided by the reference value (col. 9, l. 17-25). Thus, Mos' ratio is of the distance measured between the leading and trailing read apparatus detecting the same transition relative to the distance measured by the leading read apparatus for adjacent transitions.

Those skilled in the art will, therefore, recognize that Mos neither shows nor suggests the limitations of counting a first number of oscillations of a first oscillator on the FPGA during a predetermined time interval, counting a second number of oscillations of a second oscillator on the FPGA during the predetermined time interval, and generating a ratio between the first number and second number of oscillations, wherein the ratio is the fingerprint.

The asserted motivation for combining Mos with Erickson is conclusory and improper. There is no evidence presented that would support including Mos' magnetic reader in Erickson's FPGA. Nor is it apparent what purpose the modification would serve since Erickson appears concerned with communicating encrypted configuration data to a PLD, not authenticating data stored on magnetic medium by way of examining transition distances.

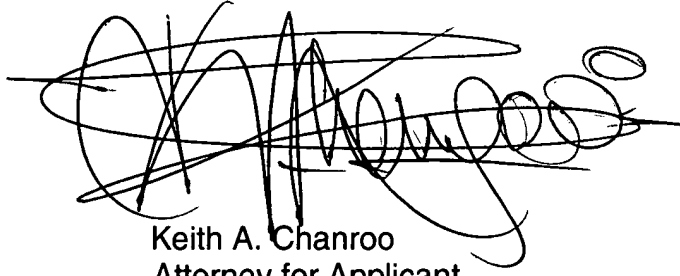
Independent claim 12 is an apparatus claim that includes the functional limitations of claim 1. Claims 2, 3, 4, and 7 depend from claim 1, and claims 13, 15, and 21 depend from claim 12. Therefore, claims 2, 3, 4, 7, 12, 13, 15, and 21 are not shown to be unpatentable over the Erickson-Mos combination.

The rejection of claims 1-4, 7, 12-13, 15 and 21 should be withdrawn because a *prima facie* case of obviousness has not been established.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Amendments and Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,

A large, stylized handwritten signature in black ink, appearing to read 'Keith A. Chanroo'.

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on November 7, 2006.

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